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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,643	07/25/2003	Shigehiro Kuge	67161-038	1395

7590 05/18/2004

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,643	KUGE ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 5* is/are rejected.

7)☒ Claim(s) *3 and 6-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *072503*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed 07-25-03 has been considered.

Specification

3. The disclosure is objected to because of the following informalities:

On page 10, line 9, the word "too" should be –to--.

On page 14, line 12, the reference "BVL-VBB" should be –VBL-VBB--.

On page 16, line 12, the reference "QN6" should read –NQ6--.

On page 17, line 23, the reference "BEQR" should be –EQR--.

On page 21, line 18, the reference "VBLL" should read –VBL--.

On page 29, line 17, the reference "SRFEXT" should be –SRFEXI—to be consistent with that in figure 10. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites the limitation "said data holding mode instruction signal " in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 4-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooshi (U.S. Patent 6,058,061).

Regarding claim 1, Ooshi teaches a semiconductor memory device comprising: a plurality of memory blocks (B1-B4 in figure 34) each having a plurality of memory cells arranged in rows and columns; a plurality of sense amplifier bands (14) arranged in correspondence to said plurality of memory blocks so as to be shared between adjacent memory blocks, each sense amplifier band including a plurality of sense amplifiers each sensing and amplifying data in a memory cell in a corresponding memory block when activated; a plurality of bit line isolation circuits (56, 62), arranged in correspondence to said plurality of sense amplifier bands, for electrically connecting, when made conductive, corresponding sense amplifier bands to corresponding memory blocks; and

a bit line isolation control circuit (which generates signals BLI1, BLI2) for setting at least the bit line isolation circuit provided for a specific memory block to be nonconductive in a standby mode of operation (column 27, lines 43-50).

Regarding claim 2, Ooshi teaches at column 27, lines 48-50, the bit line isolation control circuit maintains said plurality of bit line isolation circuits to be nonconductive in said standby mode of operation, to isolate said plurality of memory blocks from the corresponding sense amplifier bands (only a selected memory block is connected to a corresponding sense amplifier band).

Regarding claim 4, Ooshi teaches the semiconductor memory device has a normal operation mode for making data access and a data holding mode (standby state) for holding data stored in the memory cells, and said bit line isolation control circuit sets said plurality of bit line isolation circuits to be nonconductive at a standby state during activation of a refresh mode instruction signal designating said data holding mode (column 27, lines 43-50).

Regarding claim 5, Ooshi also teaches that the bit line isolation control circuit controls the bit line isolation circuits so as to electrically connect said plurality of memory blocks to the corresponding sense amplifier bands at said standby state when said data holding mode instruction signal is deactivated (column 27, lines 43-46).

Allowable Subject Matter

8. Claims 3, 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the memory device according to claim 1 further comprising the bit line isolation control circuit includes a program circuit generating a signal for specifying a selected memory block.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Komatsu (U.S. Patent 5,251,176), Watanabe (U.S. Patent 6,091,659) and Hidaka (U.S. Patent 6,563,748) teach memory blocks selectively coupled to shared sense amplifier bands.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

05-13-04

Son L. Mai
Primary Examiner
Art Unit 2818